LOGSYS – Development Environment of Embedded Systems

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1. Introduction

Systems built with programmable logic devices (FPGA, CPLD) and microcontrollers require efficient development support. Manufacturer development tools focus on their own devices and offer only a limited communication support with the application itself. The power supply of target systems is also usually left to external instruments.

For that reason, a new development environment has been created, which integrates the configuration, the communication and the power supply features in a vendor independent manner.

2. The Development Cable

The development cable connects the target system with the PC through the USB port. It provides a configuration interface, a control interface (a clock and a reset signal), a serial communication interface and a 5 V power output. Because different systems can use different voltage levels for communication, the development cable contains level shifter circuits. This flexibility enables the development cable to be easily attached to many targets.

| JTAG TDO	JTAG TCK	CLK	MOSI	Vref I/O	5 V
JTAG TDI	JTAG TMS	RST	MISO	GND	Vref JTAG

3. The User Application

The user application and the device drivers require Windows XP operating system. The user application has a customizable and well-arranged graphical interface for accessing the functions provided by the development cable.
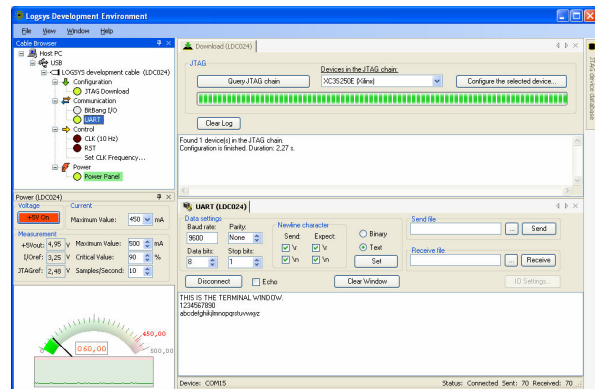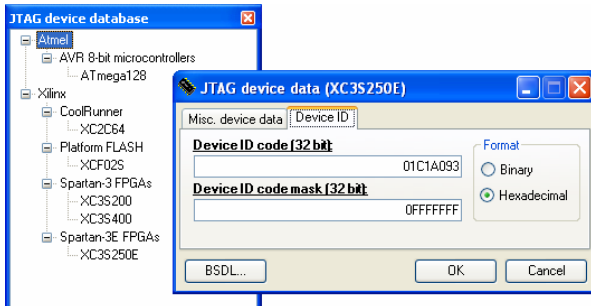

4. Configuration

The native configuration interface is the JTAG interface for configuring programmable devices.

The LOGSYS system uses the industry standard SVF file format to describe the operations on the JTAG chain. Most manufacturer development environments provide a way to create an SVF file that describes the configuration. In case of Xilinx devices, the BIT and the JEDEC files are also directly supported by the application.
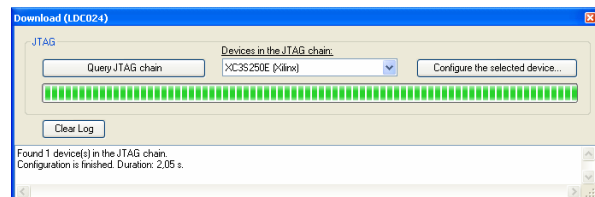
The LOGSYS configuration tool has an internal device database to manage the devices from different manufacturers in the JTAG chain. The required data can be entered manually or can be imported from BSDL files of the devices.

Thanks to the JTAG device database, JTAG chains with devices from different manufacturers can be handled without any difficulties. At the beginning of the configuration process, the devices in the JTAG chain have to be queried first. Then the user can download the configuration file to the selected device.
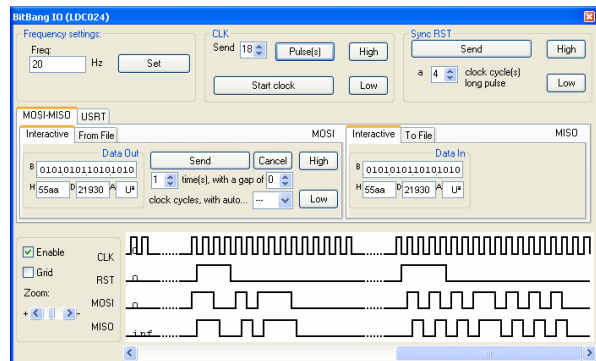
5. Communication

The development cable supports a range of synchronous and asynchronous serial communication protocols. Basically, the popular UART can be used to communicate with the target system. A virtual serial port driver has been created so the UART of the development cable can be accessed from the Windows applications. A simple terminal interface is available in the LOGSYS environment for UART communication.
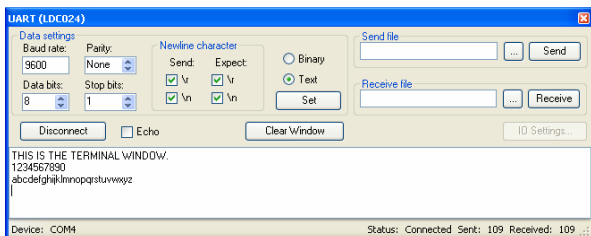
For simple tests or educational purposes a special communication mode called BitBang I/O is available. In this mode the software directly controls the clock, changes the reset and serial data out lines and samples the

serial data input at the rising or falling clock edge. Data files can be used for the I/O also.

The development cable also supports the master USRT (synchronous version of the UART), master SPI and master I^2C (SMBus) communication modes.

6. Power Supply and Measurement

USB ports have a short circuit protected 5 V power output and supply 500 mA current. Because the development cable consumes less than 30 mA current, the USB port can be used to power the target systems. The development cable has a power switch with adjustable current limits of 450 mA, 750 mA and 950 mA. Setting the current limit greater than 500 mA requires a Y-type USB cable. The voltage on all power lines and the output current are measured, and the results are displayed in the user application.

The user can control the power output and the current limit from the power panel. This interface also serves for displaying the measurement results and the history of the current consumption.